Claims:

1. Apparatus for increasing the time resolution of a clock in an electronic device; said apparatus comprising a first delay element having an input for receiving and delaying an input signal by a first amount of time to produce an output signal;

a second delay element for delaying said output signal by a predetermined fraction of a period of said clock to produce a second output signal;

a feedback path for transmitting said second output signal to said input of said first delay element and

an inverter for inverting either said output signal or said second output signal.

2. The apparatus of claim 1 wherein the first delay element comprises a programmable delay element.

3. Apparatus of claim 2 wherein said second delay element includes plural third delay elements in combination with a selector for selecting one of the plural delay elements.

4. Apparatus of claim 3 further comprising a microprocessor connected to both the selector and the programmable delay element for programming the proper delay into the programmable delay element and for selecting an output from one of said third delay elements to feed back to the input of said programmable delay.

5. Apparatus of claim 4 further comprising a delay lock loop connected to said third delay elements to cause total delay introduced by all of said third delay elements to be equal to a period of said clock.

6. Apparatus for generating a pulse width modulated (PWM) signal from a clock having lower resolution than that of said PWM signal, said apparatus comprising a first

delay element for delaying an input signal by a first predetermined amount to produce a first output signal, a second delay element for delaying said first output signal by a second predetermined amount to produce a second output signal, and a logic gate for performing a logic function with respect to said first and second outputs.

7. Apparatus of claim 6 wherein said logic gate is an OR gate or and AND gate.

8. Apparatus of claim 7 wherein said second delay element comprises plural third delay elements and a selector for selecting an output of one of said third delay elements.

9. Apparatus of claim 8 wherein said third delay elements are arranged in series such that a total delay introduce by all of said third delay elements is equal to one period of a clock, the clock also being configured to drive the first delay element.

10. Apparatus of claim 9 further comprising a delay lock loop for maintaining appropriate delays of each of said third delay elements.

11. A method of producing a Pulse Width Modulated (PWM) signal, said method comprising receiving in an OR gate a first signal and a second signal, the second signal being selected from plural third signals, each of said plural third signals being equal to a delayed version of said first signal, said delay being equal to T/n, where n is a selected one of a different integer for each of said third signals, and T is a clock signal.

12. The method of claim 11 further comprising connecting a delay lock loop to plural delay elements to generate said third signals.

13. The method of claim 11 wherein an original signal is delayed by a preprogrammed amount and subsequently by plural delays of equal value.